EE 223 Homework 4

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11/04/2018

Design of High-Swing Cascode Bias and Cascode OTA Circuit

1. Schematic and DC Operating Points of the Circuit

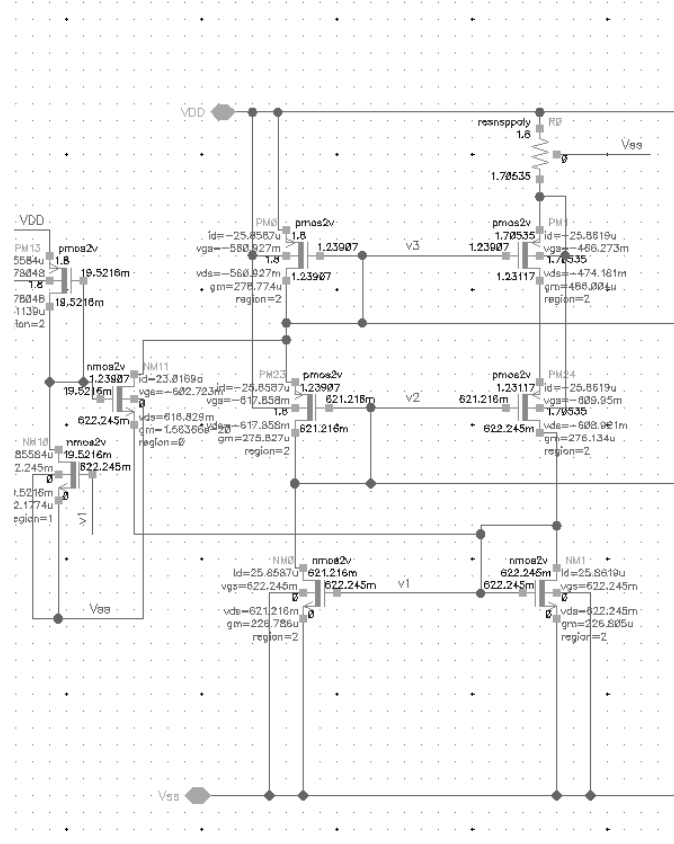


Figure 1: Start Up Circuit and Beta Multiplier DC Operating Points and Node Voltages

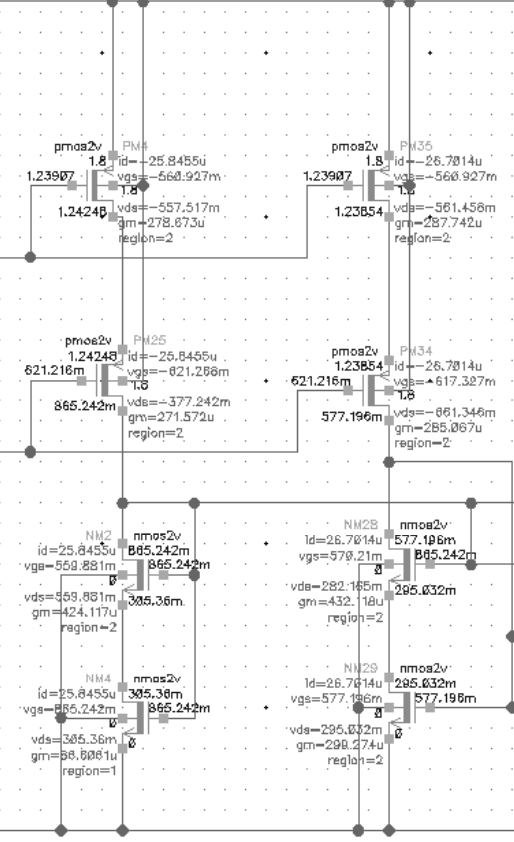


Figure 2: Nmos High Swing Current Cascode DC operating point and Node Voltage.

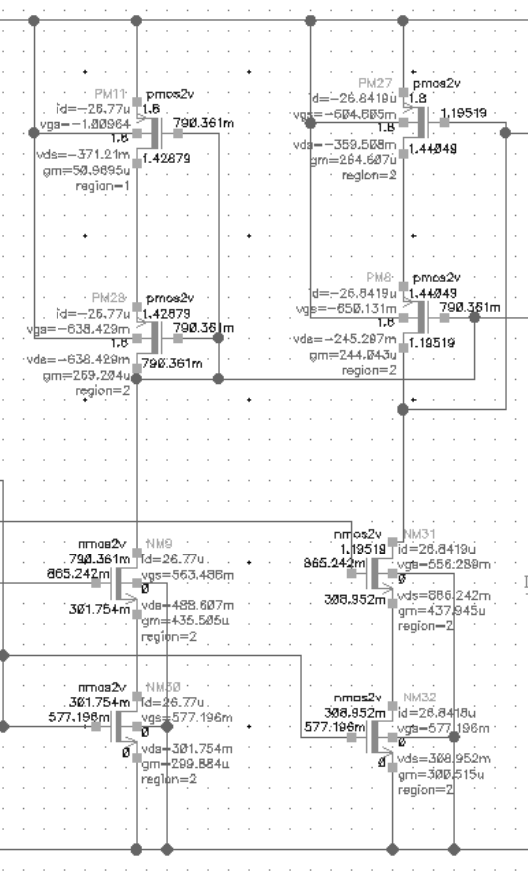
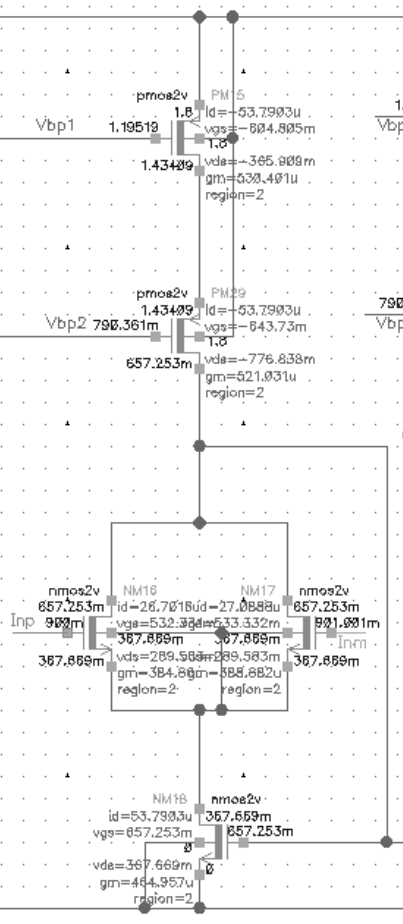


Figure 3: Pmos High Swing Current cascode DC operating Point and Node voltage.



Fiugre 4: Fully differential DC Operating point and Node voltage.

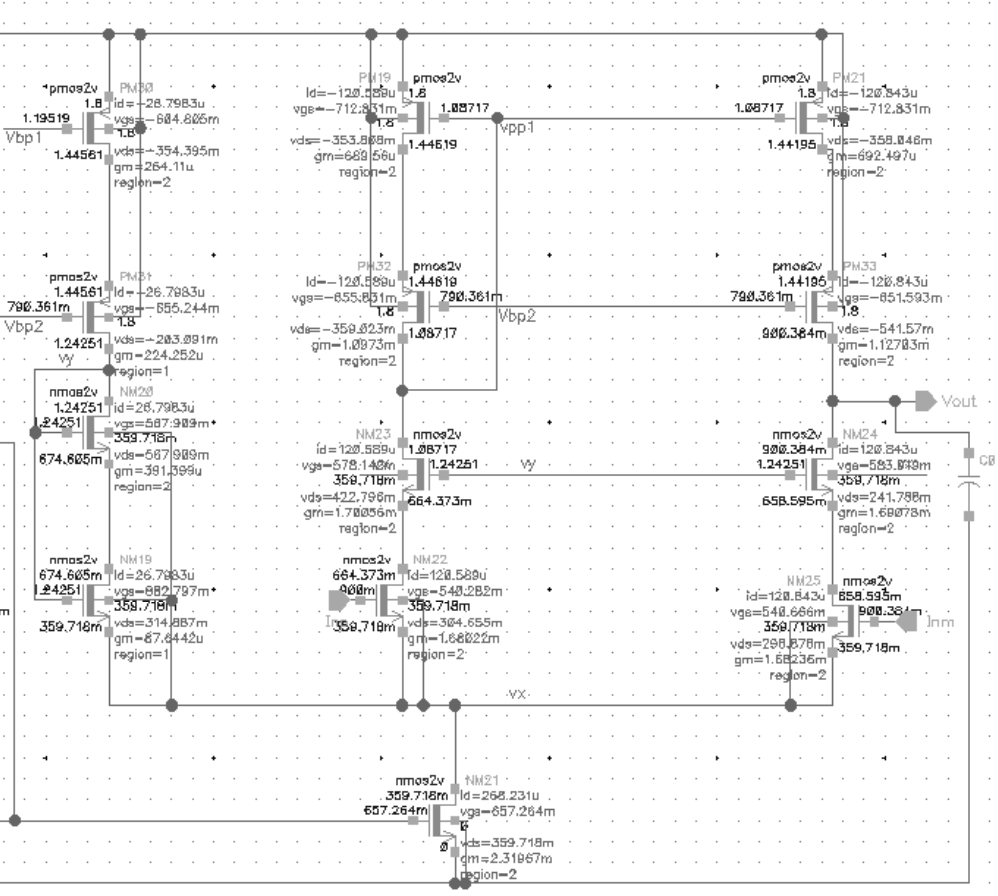


Figure 5: Operational Transconductance Amplifier DC Operating point and Node Voltage.

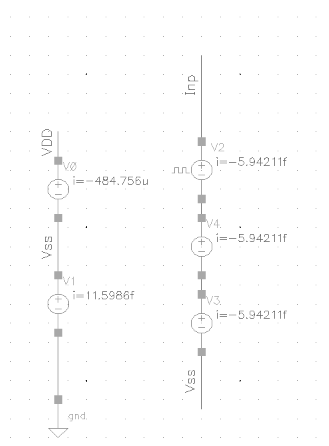


Figure 5: Circuit Power dissipation VDD= 1.8V, I=484.755uA, P=872.561uW (VDD\*I).

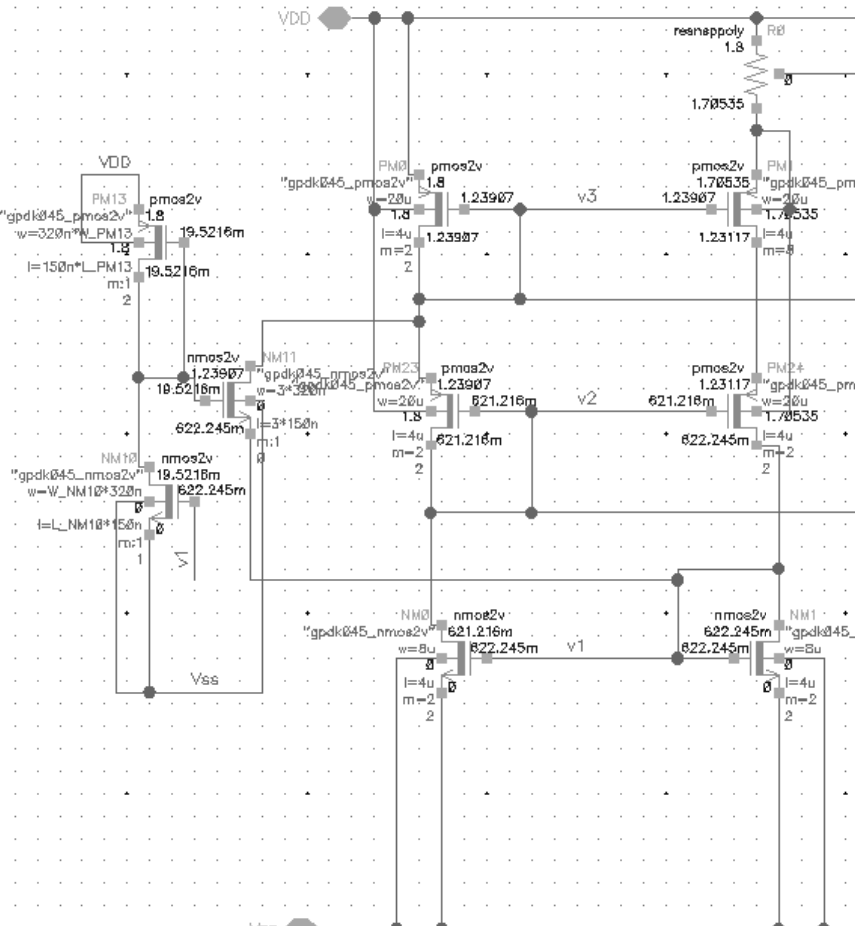


Figure 6: Start Up and Beta multiplier device size and region of operation. Where w\_pm13=1, W\_PM13 = 50, L\_NM10=2 and W\_NM10=10.

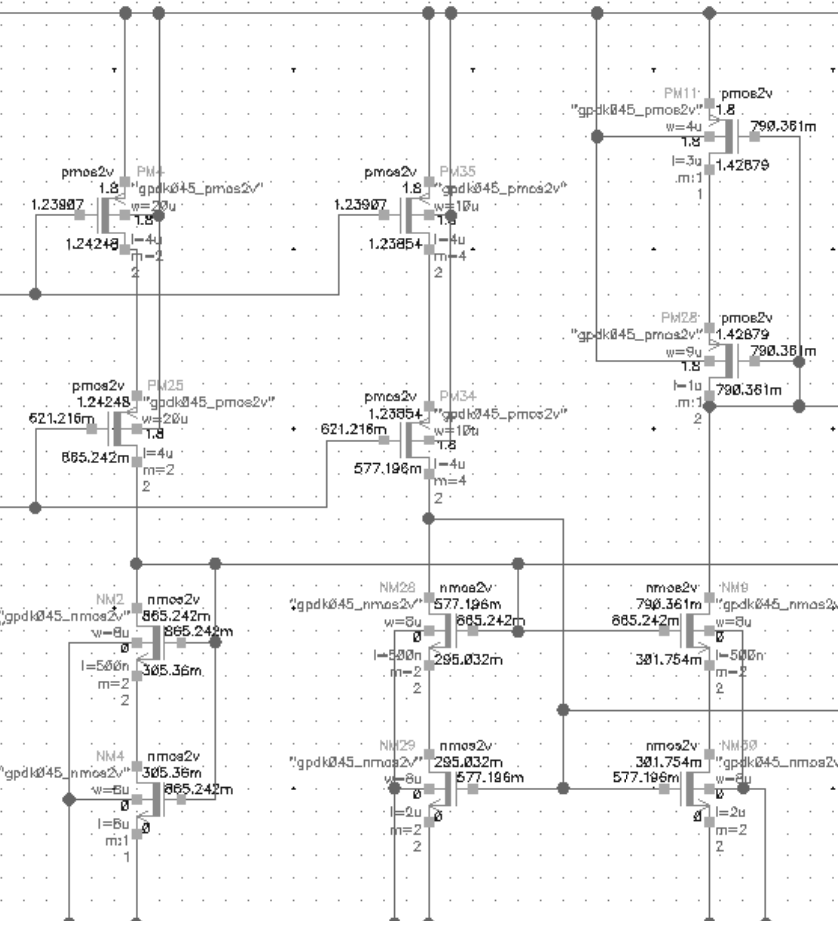


Figure 7: NMOS high swing current cascode device size and DC operating region.

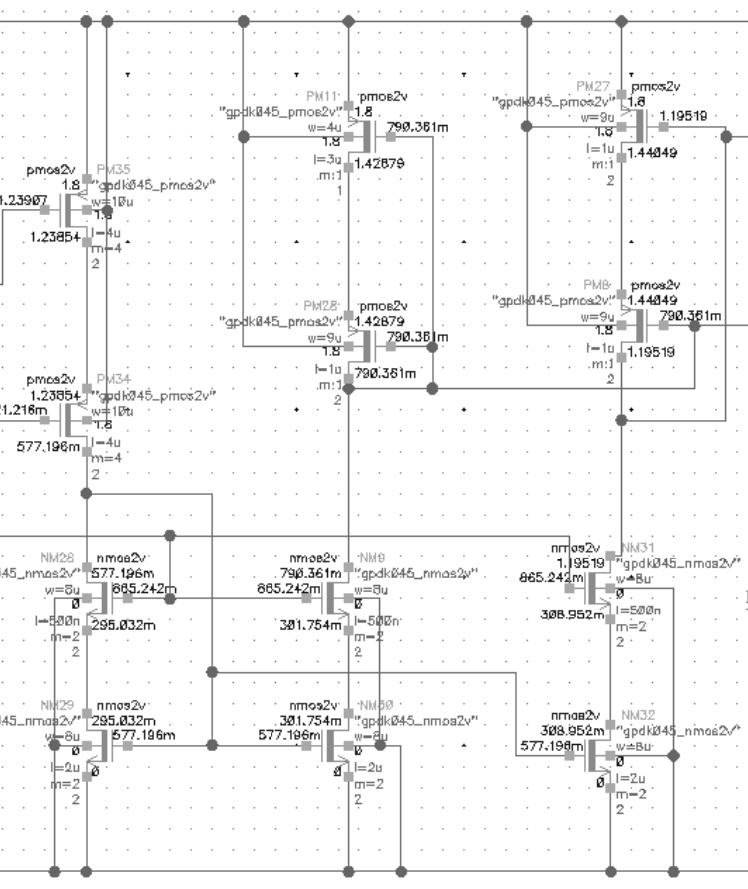


Figure 8: PMOS high swing current cascode device size and DC operating region.

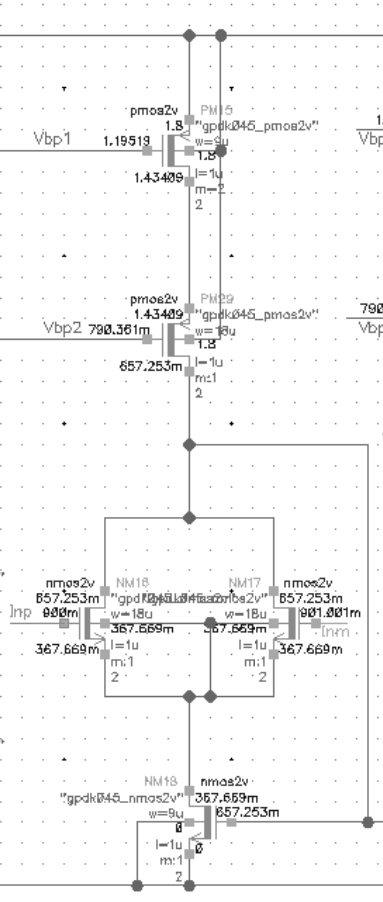


Figure 9: Fully differential circuit device size and DC operating region.

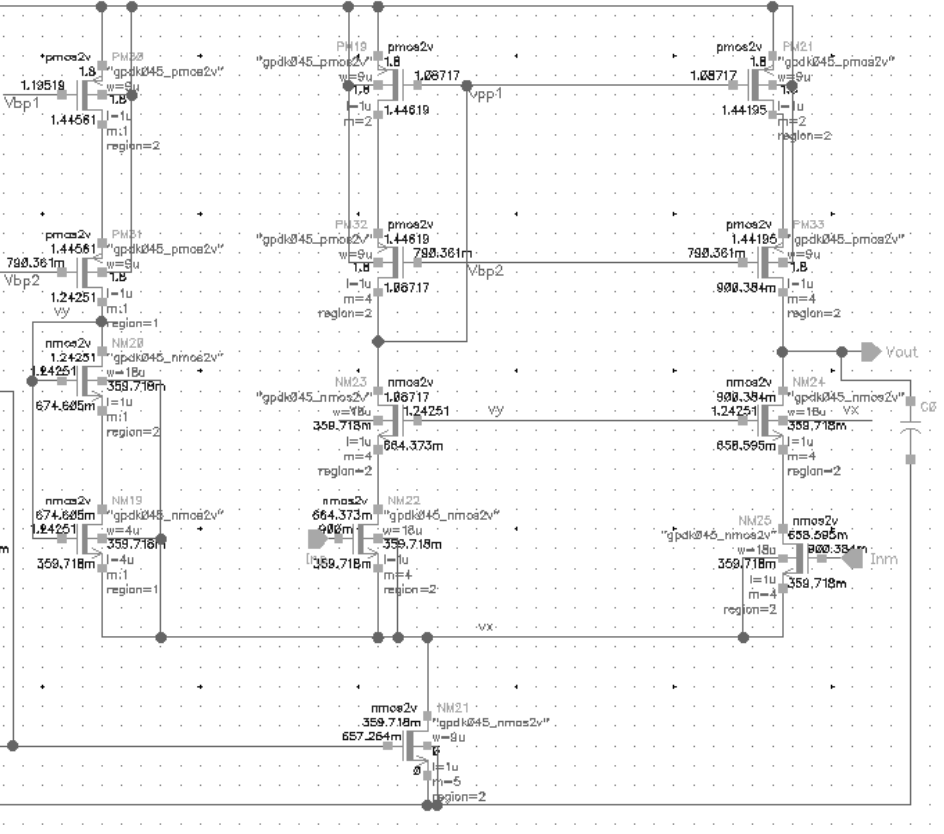


Figure 10: Operational Transconductance Amplifier devices size and DC Operating region.

1. AC Simulation and results.

Schematic

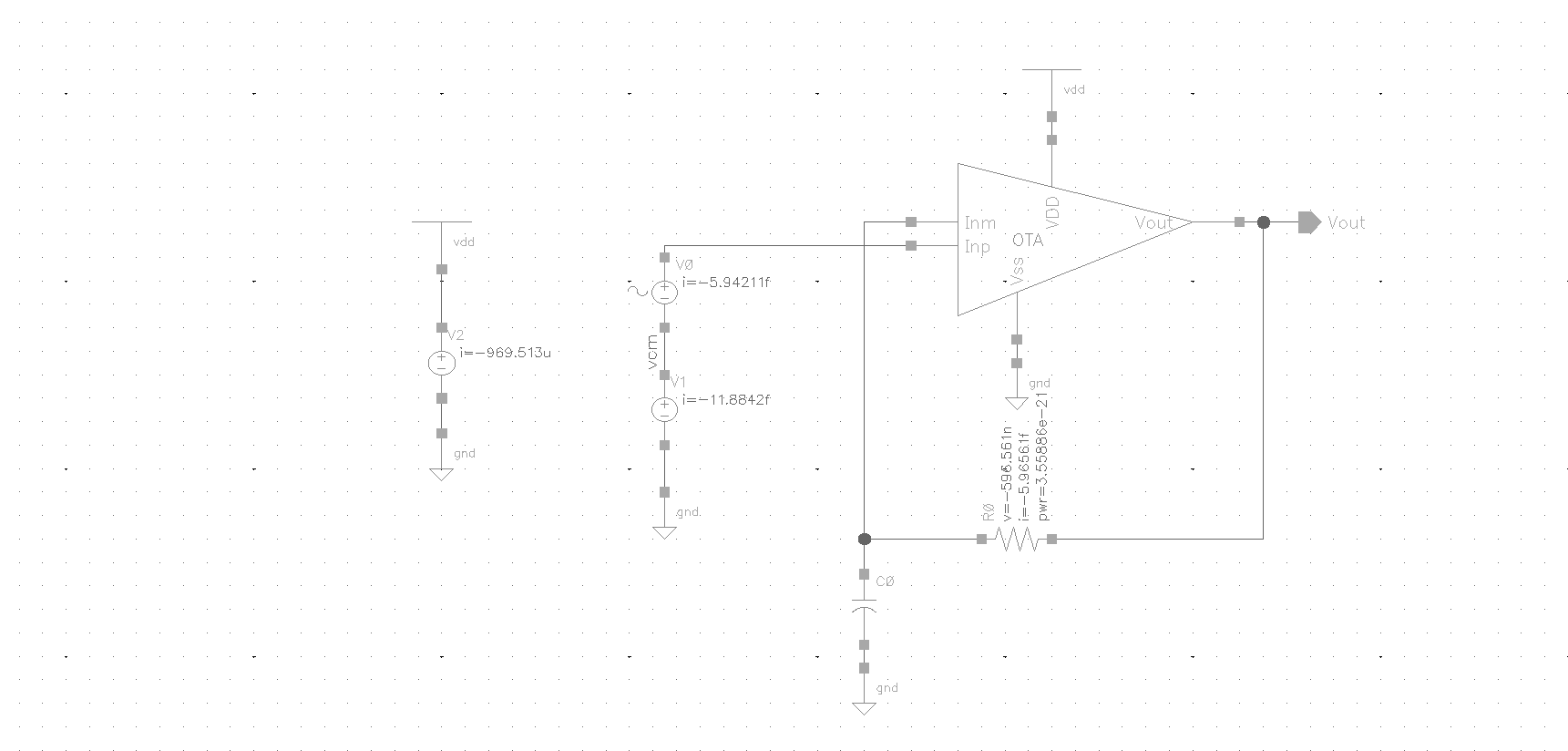


Figure 11: AC response schematic

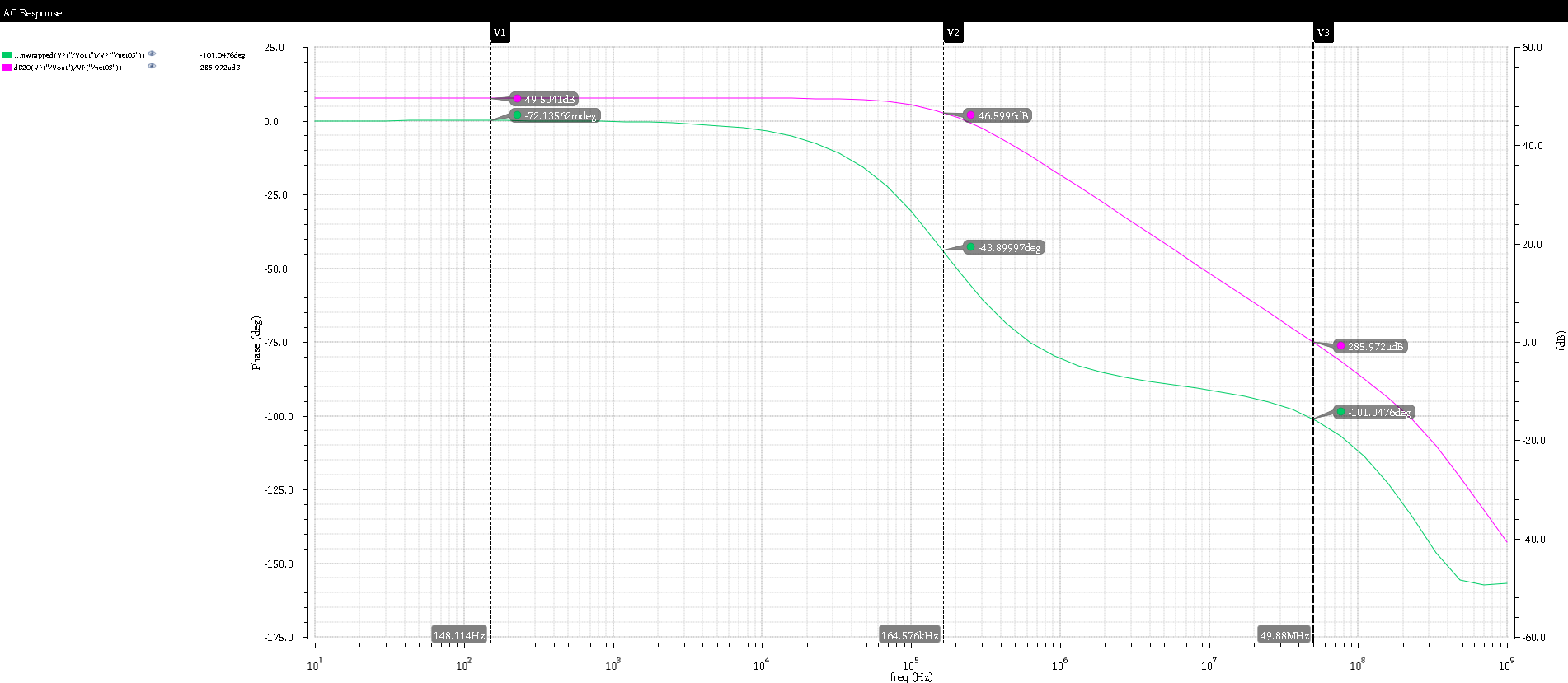


Figure 12: AC response plot

Table 1: AC response Results

|  |  |  |
| --- | --- | --- |
| Parameter | Gain[dB] | Frequency[HZ] |
| A0 | 49.501 | 0 |
| -3dB BW | 46.59 | 164.57K |
| Wu | 0 | 49.88M |
| A0\*-3dB BW |  | 49.1182M |

1. Transient simulation of Buffer configuration

Schematic

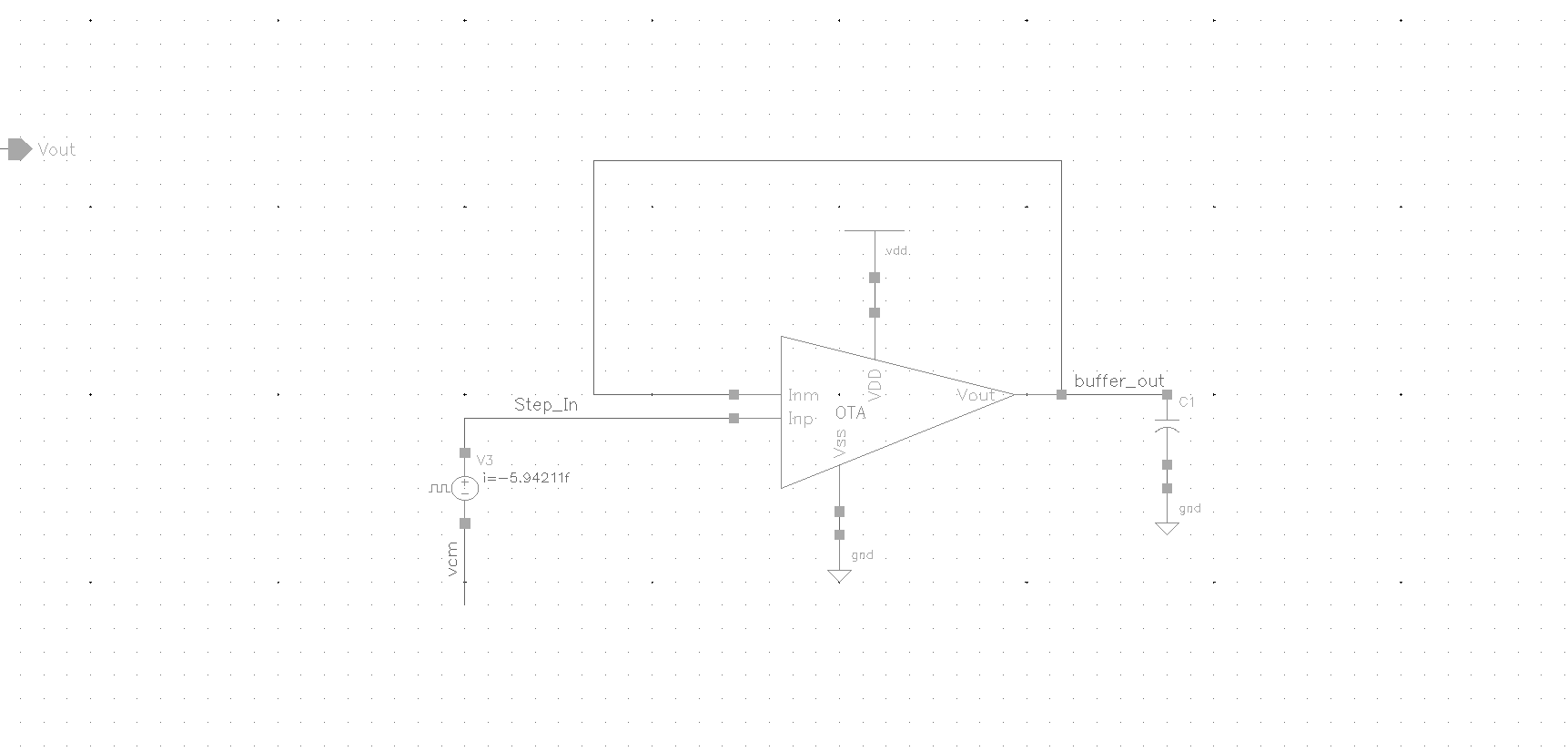


Figure 13: Unity gain configuration circuit.



Figure 14: Transient Response of the Unity gain configuration (red trace is output, and green is input).